

Amendments to the Claims:

Please cancel claims 40-42. Please amend claims 43-46 and 52 as follows.
Following is a complete listing of the claims pending in the application, as amended:

1-33. (Canceled)

34. (Original) A microelectronic device, comprising:
a workpiece including a substrate, a plurality of active areas in the substrate, and
a dielectric layer over the active areas;
a plurality of bit line contacts in the dielectric layer contacting first portions of the
active areas;
a plurality of cell plugs in the dielectric layer contacting second portions of the
active areas; and
a bit line structure embedded in an upper portion of the bit line contacts and
portions of the dielectric layer between the bit line contacts, the bit line
structure comprising an elongated conductive bit line and a dielectric
spacer between the conductive bit line and cell plugs adjacent to the bit
line.

35. (Original) The device of claim 34, further comprising a liner between the
bit line and the dielectric spacer.

36. (Original) The device of claim 34 wherein:
the bit line comprises tungsten; and
the device further comprises a tungsten nitride barrier layer between the
tungsten bit line and the spacer.

37. (Original) The device of claim 34 wherein:
the bit line comprises copper; and
the device further comprises a tantalum barrier layer between the copper bit line
and the spacer.

38. (Original) The device of claim 34 wherein:
the dielectric layer has a top surface; and
the bit line has a top surface coplanar with the top surface of the dielectric layer.

39. (Original) The device of claim 34 wherein:
the device further comprises a shallow trench isolation structure adjacent to the
first portion of the active areas; and
the conductive bit line is superimposed over a portion of the shallow trench
isolation structure but not over the first active area.

40-42. (Cancelled)

43. (Currently Amended) ~~The device of claim 41 wherein:~~

~~the bit line~~ A microelectronic device, comprising:
a workpiece including a substrate, a plurality of active areas in the substrate, and
a dielectric layer over the active areas, the dielectric layer having an upper
surface;
a plurality of bit line contacts in the dielectric layer contacting first portions of the
active areas;
a plurality of cell plugs in the dielectric layer contacting second portions of the
active areas;
a conductive, elongated bit line embedded in an upper portion of the bit line
contacts and portions of the dielectric layer between the bit line contacts,
wherein the bit line comprises copper and extends between cell plugs;
and
a dielectric spacer between the bit line and the cell plugs; and
a liner between the bit line and the dielectric spacer, wherein the liner comprises
a tantalum barrier layer.

44. (Currently Amended) The device of claim 430 wherein:
the dielectric layer has a top surface; and
the bit line has a top surface coplanar with the top surface of the dielectric layer.

45. (Currently Amended) The device of claim 430 wherein:
the device further comprises a shallow trench isolation structure adjacent to the
first portion of the active areas; and
the conductive bit line is superimposed over a portion of the shallow trench
isolation structure but not over the first active area.

46. (Currently Amended) A computer, comprising:
a bus;
a central processing unit coupled to the bus; and
a memory device coupled to the bus, the memory device having a cell
comprising—:
a plurality of active areas in the substrate, and a dielectric layer over the
active areas;
a plurality of bit line contacts in the dielectric layer contacting first portions
of the active areas;
a plurality of cell plugs in the dielectric layer contacting second portions of
the active areas; and
a bit line structure embedded in an upper portion of the bit line contacts
and portions of the dielectric layer between the bit line contacts, the
bit line structure comprising an elongated conductive bit line and a
dielectric spacer between the conductive bit line and cell plugs
adjacent to the conductive bit line.

47. (Original) The computer of claim 46, further comprising a liner between
the bit line and the dielectric spacer.

48. (Original) The computer of claim 46 wherein:
the bit line comprises tungsten; and
the computer further comprises a tungsten nitride barrier layer between the
tungsten bit line and the spacer.

49. (Original) The computer of claim 46 wherein:
the bit line comprises copper; and
the computer further comprises a tantalum barrier layer between the copper bit
line and the spacer.

50. (Original) The computer of claim 46 wherein:
the dielectric layer has a top surface; and
the bit line has a top surface coplanar with the top surface of the dielectric layer.

51. (Original) The computer of claim 46 wherein:
the computer further comprises a shallow trench isolation structure adjacent to
the first portion of the active areas; and
the conductive bit line is superimposed over a portion of the shallow trench
isolation structure but not over the first active area.

52. (Currently Amended) A computer, comprising:
a bus;
a central processing unit coupled to the bus; and
a memory device coupled to the bus, the memory device having a cell
comprising—:
a workpiece including a substrate, a plurality of active areas in the
substrate, and a dielectric layer over the active areas, the dielectric
layer having an upper surface;
a plurality of bit line contacts in the dielectric layer contacting first portions
of the active areas;

a plurality of cell plugs in the dielectric layer contacting second portions of the active areas;

a conductive, elongated bit line embedded in an upper portion of the bit line contacts and portions of the dielectric layer between the bit line contacts, the bit line extending between cell plugs; and

a dielectric spacer between the conductive bit line and cell plugs adjacent to the conductive bit line.